Claims 16-28 are pending in the application. These claims were rejected as follows:

Claims / Section	35 U.S.C. Sec.	References / Notes
16-28	§102(a) Anticipation	• Linke, et al. (U.S. Patent No. 5,960,188).

Applicant has provided discussion for distinguishing the claims of the present invention from the disclosure of Linke and respectfully request reconsideration of the application in light of the following remarks..

Applicant's use of reference characters below is for illustrative purposes only and is not intended to be limiting in nature unless explicitly indicated.

35 U.S.C. §102(a), CLAIMS 16-28 ANTICIPATION BY LINKE

1. Linke does not anticipate independent claims 16 and 28 of the present invention because it fails to teach or suggest the element of a second series of steps being executed in an accelerated operating mode which is matched to the evaluation, where the second series of method steps are stipulated by markers inserted into the first series of method steps.

In the OA, on pp. 2-3, under numbered paragraph 3, the Examiner read the elements of Linke onto the elements of the independent claims as follows:

> The Linke et al. reference teaches a simulation system of a micro controller including the peripherals (Col. 15 lines 32-50 note lines 33 and 34 with the phrase cycle-based simulator being developed for the purpose of testing embedded software on a microcontroller), predetermined signal patterns (Figure 1 and Col. 10 lines 9-27 note the discussion of the output information this would be in the form of a stimulus, which is the functional equivalent of a signal

> pattern), a first series of steps and a second series of steps and markers (Figure 3A item 38, Figure 4 items 100, and 101, Col. 11 lines 53-67 and Col. 12 lines 1-4 note the phrase on line 55 of column 11. The method begins by first asking (100) whether the Change Marker data is zero, or some other value that refers to the in which a New Level, functional equivalent of Step, or New Strength, functional equivalent of a new pattern, was asserted functional equivalent of "INPUT", on the wire.) a control unit (Col. 15 line 42 the SUN SPARCstation is the control unit for the simulation) with clock cycle accuracy (Col. 5 lines 45-61), and program instruction interrupted by an instruction set simulator (Col. 4 lines 61-67 and Col. 5 lines 1-18).

Applicant respectfully disagrees with this characterization of Linke, and notes that the element of operating in an accelerated operating mode is completely absent in the disclosure of Linke and in the Examiner's reading of Linke onto the claim elements of the independent claims in the application.

The independent claims of the application identify an accelerated operating mode for operating the second series of method steps, this second series of method steps being stipulated by markers inserted into the first series of method steps. The markers in the first series of method steps triggering the second series of method steps in an interrupt manner.

As best as can be determined, the Examiner is equating the Change Marker data of Linke with the markers of the present invention. However, the Change Marker data in Linke does not serve as a trigger for processing a second series of method steps in an accelerated operating mode. Rather, Linke utilizes the Change Marker simply as a status update mechanism. In the portions of Linke cited by the Examiner (11/53 – 12/4), Linke states:

> FIG. 4 is a flowchart of a method to get the current value of a wire. It is initiated by an Input Node at the encapsulating Module's request. The method begins by first asking(100) whether the Change Marker data is zero, or some other value that refers to the cycle in which a New Level or New Strength was asserted on the wire. If the change marker is zero, then the Wire's Current Level and Current Strength are up to date, and can be immediately reported(103). If the change marker is nonzero, that is, if it identifies a cycle, the next step (101) is to determine whether the Wire's value changed in an earlier cycle. If the Change Marker is non-zero and refers to the current cycle, then the value of Current Level and Current Strength still represent the current value of the wire. Otherwise, the New Level and New Strength need to be synchronized. This is done in step (102) by copying the New Level to Current Level, copying New Strength to Current Strength and setting the Change Marker to zero. Then the Wire's Current Level and Current Strength can be reported (103).

In other words, the Change Marker is zero, this indicate that the current level and strength are currently up to date, but if it is non-zero, then a synchronization of the new level and strength needs to be effected before reporting the values. However, there is no discussion about the markers being used to trigger operation of a second series of steps in an accelerated operating mode.

The operation in an accelerated operating mode is an important feature of the present invention. By way of example, in non-accelerated operational mode, a serial interface, over several (simulated) clock cycles, converts data bit-by-bit into an output signal. Thus, simulation time is passing as this occurs. However, at some point, one wants to investigate, for example, the contents of a buffer into which the serial data is moving—however, if the accelerated mode is not entered into, then the mere investigation into the contents of the buffer affects the

simulation timing. Therefore, one enters the accelerated operation mode to query the contents of the buffer, display it, or perform other operations on it. While in the accelerated operation mode, the simulation time does not pass—therefore, the investigation of the buffer contents does not interfere with the timing in the simulation. Of course, the hardware clock physically connected to the CPU continues to operate or the CPU would not run, but the real "hardware" clock of the CPU is, in fact, decoupled from the simulation clock, as described by the Specification.

Such a mechanism is neither taught or suggested by Linke. Linke deals with a simulation involving two types of simulated objects: a node (a hardware output's driver and hardware input's receiver), and a wire (the interconnection between two devices). The focus of Linke is directed to managing new and current values of output signals and the identification of a cycle associated with a particular change (see Linke, Abstract), but does not address a system capable of an accelerated mode and non-accelerated mode for executing instructions.

Applicant further notes that the portion of Linke that the Examiner relies on for disclosing the elements related to an interrupt of the present invention relate to Linke's discussion of the prior art at 4/61-5/18. While a discussion of prior art in a reference can serve as anticipating disclosure, in the case of the Linke reference, a disclosure is lacking that provides the logical relationship between the elements discussed as prior art and the elements that the Examiner is relying upon in the descriptive portion of the Linke invention for aspects such as the markers and the first/second series of steps. The discussion of Linke at 4/61-5/18 does not convey the elements of a first series of instructions operating in a

non-accelerated mode with a second series of instructions operating in an accelerated mode, but rather simply identifies the overall need of having a simulator capable of handling a large number of clock cycles per second. It does not teach or suggest the need for both an accelerated mode and a non-accelerated mode. It is necessary to show by the prior art not only the claimed elements, but also the claimed interrelationships of the elements—Linke fails not only to teach all of the elements of the independent claims, but particularly fails to teach the interrelationships between the elements as claimed.

For these reasons, the Applicant asserts that the amended claim language clearly distinguishes over the prior art, and respectfully request that the Examiner withdraw the §102(a) rejection from the present application. In the event the rejection is maintained, the Applicant respectfully requests that the Examiner clearly indicate Linke's disclosure related to an accelerated operating mode for a second series of method steps and its relationship to markers inserted into the first series of method steps.

CONCLUSION

Inasmuch as each of the objections have been overcome by the amendments, and all of the Examiner's suggestions and requirements have been satisfied, it is respectfully requested that the present application be reconsidered, the rejections be withdrawn and that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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